Registration No : | | | | | | | | | | |

Total Number of Pages : 03

B.Tech
RCS5D001

5th Semester Reg/Back Examination: 2024-25
Advanced Computer Architecture
CST, CSE
Time : 3 Hour
Max Marks : 100
Q. Code : R017

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** (2 x 10)

a) What is meant by anti-dependence? How is it removed?
b) Define RAW, WAW, WAR hazards.
c) Is VLIW a RISC or CISC? Justify.
d) How many Floating-point registers are there in the Floating-Point Unit of SPARC?
e) What are the problems faced in superscalar architecture?
f) A four-stage pipeline has stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, calculate the total time taken to process 1000 data items on this pipeline.
g) Name any two static connection network and dynamic connection network.
h) Define the term "Virtual Memory ".
i) How can an interleaved memory mechanism be used to improve the processing speed of a computer system?
j) Given page reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6
Find the number of page faults for optimal page replacement algorithm

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** (6 × 8)

a) Consider a 4-stage pipeline that consists of Instruction Fetch(IF), Instruction Decode(ID),Execute(Ex) and Write Back(WB) stages. The times taken by these stages are 50 ns,60ns,110ns and 80ns respectively. The pipeline registers are required after every pipeline stage, and each of these pipeline registers consumes 10ns delay. What is the speedup of the pipeline under ideal conditions compare to the corresponding non-pipelined implementation?

b) Illustrate the architectural features of VLIW processor with timing diagram. How does it differ from superscalar processor?

c) Whether array processor is same as vector processor? Justify your answer.

d) Which memory architecture is scalable UMA or NUMA? Justify.

e) In the context of multistage networks, construct a 64-input Omega network using 4 X 4 switch modules in multiple stages. How many permutations can be implemented directly in a single pass through the network without blocking?

f) Differentiate between Super scalar architecture and Super pipelined architecture.

g) Consider a 7-stage pipeline processor. In the first stage, instruction is fetched. In the second stage, the instruction is decoded as well as branch target address is computed for branch instructions. In the third stage, the branch outcome is evaluated. Assume 25% of all branches are unconditional branches. Of all the conditional branches, on the average 80% tum out to untaken. Compute the average pipeline stall cycles per branch instruction under pipeline stall, conditional taken, conditional untaken, delayed branch schemes. Ignore structural and data hazards. For delayed branch scheme assume that suitable successor is always found.

h) Distinguish between typical RISC and CISC processor architectures.

i) Compare and contrast static interconnection network and dynamic interconnection network.

j) Explain with suitable example LRU page replacement algorithm. Given page reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6
Find the number of page faults for LRU page replacement algorithm

k) What is cloud computing? Explain its characteristics and features.

l) Discuss the various techniques available for reducing cache miss penalty. Suppose that in 1000 memory reference there are 50 misses in the first level cache and 20 misses in the second level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 100 clock cycles the hit time of the L2 cache is 10 clock cycles. The hit time of L1 is 1 clock cycle and there are 2 memory references per instruction. What is the average memory access time?

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Define the term pipelining? Explain different types of hazards that occur in instruction pipeline and how to handle them. **(16)**
Consider a 4-stage pipeline that consists of Instruction Fetch(IF), Instruction Decode(ID),Execute(Ex) and Write Back(WB) stages. The times taken by these stages are 50 ns,60ns,110ns and 80ns respectively. The pipeline registers are required after every pipeline stage, and each of these pipeline register consumes 10ns delay. What is the speedup of the pipeline under ideal conditions compare to the corresponding non-pipelined

implementation?

Q4 Describe Flynn's classification of computer architecture. With a neat diagram, describe the three shared memory multi-processor models. **(16)**

Q5 Compare buses, crossbar switches, and multistage networks for building a multiprocessor system with n processors and m shared-memory modules. Assume a word length of w bits and that 2 X 2 switches are used in building the multistage networks. The comparison study is carried out separately in each of the following four categories: **(16)**

(a) Hardware complexities such as switching, arbitration, wires, connector or cable requirements.

(b) Minimum latency in unit data transfer between the processor and memory module.

(c) Bandwidth range available to each processor.

(d) Communication capabilities such as permutations, data broadcast, blocking handling,etc.

Q6 What is Locality of Reference? Explain about Cache memory in detail. Illustrate the mapping process involved in transformation of data from main to Cache memory. A computer has a 4 GByte memory with 32 bit word sizes. Each block of memory stores 32 words. The computer has a direct-mapped cache of 64 blocks. The computer uses word level addressing. What is the address format? If we change the cache to an 8-way set associative cache, what is the new address format? **(16)**