Registration No.: | | | | | | | | | | |

Total Number of Pages: 02

Course:B.Tech
Sub_Code:REC5D006

5th / 7th Semester Regular/Back Examination: 2024-25
SUBJECT: Digital VLSI Design
BRANCH(S): AEIE, CSE, EEE, ELECTRICAL, ECE, ETC, IT, MMEAM, MECH
Time: 3 Hours
Max Marks: 100
Q.Code: R399

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Why modularity is important in designing VLSI Circuits?
b) Differntiate between Lambda and Micron design rules.
c) Why constant voltage scaling is preferred?
d) Why Noise Margin of CMOS is better than Resistive Load Inverter?
e) Draw a two input NOR gate using dynamic logic.
f) What is the most important advantage of CMOS transmission gate compared to pass transistor logic.
g) What are the different types of fault models?
h) Why LFSR is used in output response analyzer?
i) Why SRAM is used in cache memory?
j) Draw a three input AND gate using pass transistor logic.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Differentiate between Regularity, Modularity, and Locality.
b) Derive the MOSFET current equation for Linear region of operation.
c) Sketch the 4:1 multiplexer using Transmission gates.
d) What do you mean by MOSFET scaling? Show how the MOSFET parameters (power, area, current density, doping densities) are scaled in constant voltage scaling.
e) Draw a JK Flipflop using static CMOS Logic.
f) Why cascading is not preferred in dynamic CMOS logic?
g) Create a circuit which will explain the Ad Hoc Testable Design Techniques.
h) Draw and explain the Scan-Based Techniques for testing of sequential circuits.

i) Draw and explain the operation of 1T DRAM Cell. Why DRAM is not preferred in high-speed logic design?

j) Draw the stick diagram of the Boolean function Y = AB + CD (E + F).

k) Draw the half adder circuit using Pass Transistor Logic.

l) Describe the operations of Flash memory with proper diagram.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 In CMOS inverter V_{dd} = 5V. The output load capacitance is 1 nF. The nMOS transistor parameters are given as $\mu_n C_{ox}$ = 20 μA/ V^2, $(W/L)_n$ = 10, $V_{T,n}$ = 1.0 V. Calculate the delay time when output is falling from 4.7 V to 1 V. **(16)**

Q4 Write and draw all the steps needed to fabricate CMOS n-well Process. **(16)**

Q5 Draw a edge triggered D Flipflop using CMOS transmission gates. **(16)**

Q6 Explain the signature analysis technique used in output response analyzer of Built in self-Test (BIST) technique with taking an example of 5-bit Linear Feedback Shift Register (LFSR). **(16)**