Registration No :

Total Number of Pages : 03

Course: B.Tech
Sub_Code: RCS5D001

5th Semester Regular/Back Examination: 2022-23
SUBJECT : Advanced Computer Architecture
BRANCH(S): CSE, CST
Time : 3 Hour
Max Marks : 100
Q.Code : L358

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) What is Instruction Level Parallelism?
b) Compare SRAM with DRAM.
c) What do you mean by Cache coherence?
d) What are the issue policies for superscalar instructions?
e) How overlapped CPU and I/O operations are performed in computer system? Explain with example.
f) State Amdahl's low and explain.
g) How many Floating-point registers are there in the Floating-Point Unit of SPARC?
h) What is loop unrolling?
i) What is the various Page Replacement Algorithms used for Page Replacement?
j) Name two differences between logical and physical addresses.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Name and explain the different network topologies used in interconnection network architecture.
b) Distinguish between typical RISC and CISC processor architectures.
c) Consider a 7-stage pipeline processor. In the first stage, instruction is fetched. In the second stage, the instruction is decoded as well as branch target address is computed for branch instructions. In the third stage, the branch outcome is evaluated. Assume 25% of all branches are unconditional branches. Of all the conditional branches, on the average 80% tum out to untaken. Compute the average pipeline stall cycles per branch instruction under pipeline stall, conditional taken, conditional untaken, delayed branch schemes. Ignore structural and data hazards. For delayed branch scheme assume that suitable successor is always found.
d) Assume a cache miss penalty is 100 clock cycles, and all instructions take 1.0 clock cycles. Let the average miss rate is 2%, there is an average of 1.5 memory references per instructions, and the average number of cache misses per 1000 instructions is 30. What is the impact on the performance and calculate the impact using both misses per instruction and miss rate?
e) What do you mean by Speed-Up of pipeline? Derive equations of Speed-Up and Efficiency for Pipeline, Super pipeline, and Super scalar architecture.
f) What is a Pipeline Hazard? How is control hazard detected and resolved? Explain with example.

g) With respect to dependencies between the instructions, discuss the following with example: (i) Data dependency (ii) Control dependency (iii) Resource dependency

h) What is virtual memory? How is a logical address mapped to physical address in virtual concept? Explain with example and diagram.

i) Discuss the various techniques available for reducing cache miss penalty. Suppose that in 1000 memory reference there are 50 misses in the first level cache and 20 misses in the second level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 100 clock cycles the hit time of the L2 cache is 10 clock cycles. The hit time of L1 is 1 clock cycle and there are 2 memory references per instruction. What is the average memory access time?

j) Distinguish between UMA and NUMA architecture.

k) Three devices A, B, and C are connected to the bus of a computer. I/O transfers for all the devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being services. Suppose different ways in which this can be accomplished in each of the following cases:

i) The computer has one interrupt request line.

ii) Two interrupt request line. INTR 1 and INTR2 are available with INTR1 having higher priority. Specify when and how interrupts are enables and disable in each case.

l) Write short notes on cloud computing.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Describe Flynn's classification of computer architecture. Compare the features of Array Processor and Vector Processors. **(16)**

Q4 A superscalar processor has 5 issue slots which can be filled up in a single clock cycle. During execution of a certain application consisting of 1000 instructions the following are observed: **(16)**
10% of the instructions were issued by filling up exactly 1 issue slot only, 20% of the instructions were issued by filling up exactly 2 issue slots only, 20% of the instructions were issued by filling up exactly 3 issue slots only, 48% of the instructions were issued by filling up exactly 4 issue slots only, and the remaining instructions were issued by filling up all the slots. But due to some reason it was found that a total of 500 clock cycles were consumed while issuing all these 1000 instructions. Find out the speedup factor in issuing instructions when there is zero vertical waste as compared to with vertical waste in the above-mentioned scenario.

Q5 What are the different types of Interconnection network used in computer architecture? Compare and contrast between static networks and dynamic networks. **(16)**

Q6 Discuss in detail the working of set associative mapped cache with four blocks per set with relevant data. A block-set associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 bocks, each consisting of 128 words. **(16)**
i) How many bits are there in the main memory address?
ii) How many bits are there in each of the TAG, SET and WORD fields?