Registration No: | | | | | | | | | | |

Total Number of Pages: 02

Course: B.Tech
Sub_Code: RCS5D001

5th Semester Regular / Back Examination: 2023-24
SUBJECT: Advanced Computer Architecture
BRANCH(S): CSE, CST
Time: 3 Hour
Max Marks: 100
Q.Code : N167

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) What are the main components of a microcontroller?
b) What do you mean by Spatial and Temporal locality of reference?
c) Define Cache coherence problem.
d) How many Floating point registers are there in the Floating Point Unit of SPARC?
e) What is a Delayed branch? How does it improve the Performance of pipeline architecture?
f) Differentiate between Address space and Memory space.
g) A CPU generates 32-bit virtual addresses. The page size is 4kB. The processor has a TLB which can hold a total of 256 page table entries. The TLB is an 8-way set associative. Calculate the TLB tag size.
h) What are the types of vector processor?
i) Write any two differences between Superscalar architecture and Super pipelined architecture.
j) What are the disadvantages of using symmetric shared memory?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Distinguish between typical RISC and CISC processor architectures.
b) Consider a 7-stage pipeline processor. In the first stage, instruction is fetched. In the second stage, the instruction is decoded as well as branch target address is computed for branch instructions. In the third stage, the branch outcome is evaluated. Assume 25% of all branches are unconditional branches. Of all the conditional branches, on average 80% tum out to be untaken. Compute the average pipeline stall cycles per branch instruction under pipeline stall, conditional taken, conditional untaken, delayed branch schemes. Ignore structural and data hazards. For delayed branch scheme assume that suitable successor is always found.
c) Name and explain the different network topologies used in interconnection network architecture.
d) Explain with suitable example LRU page replacement algorithm. Given page reference string: 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6
Find the number of page faults for LRU page replacement algorithm

e) Consider a 4-stage pipeline that consists of Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex) and Write Back (WB) stages. The times taken by these stages are 50 ns, 60ns, 110ns, and 80ns respectively. The pipeline registers are required after every pipeline stage, and each of these pipeline register consumes 10ns delay. What is the speedup of the pipeline under ideal conditions compare to the corresponding non-pipelined implementation?

f) Suppose that in 1000 memory reference there are 50 misses in the first level cache and 20 misses in the second level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 100 clock cycles the hit time of the L2 cache is 10 clock cycles. The hit time of L1 is 1 clock cycle and there are 2 memory references per instruction. What is the average memory access time?

g) What is virtual memory? How is a logical address mapped to physical address in virtual concept? Explain with example and diagram.

h) Illustrate the architectural features of VLIW processor with timing diagram. How does it differ from superscalar processor?

i) What is cloud computing explain its characteristics and features?

j) Discuss the various techniques available for reducing cache miss penalty.

k) Distinguish between UMA and NUMA architecture.

l) Three devices A, B, and C are connected to the bus of a computer. I/O transfers for all the devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being services. Suggest different ways in which this can be accomplished in each of the following cases:

i) The computer has one interrupt request line.

ii) Two interrupt request line. INTR1 and INTR2 are available with INTR1 having higher priority. Specify when and how interrupts are enables and disable in each case.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Explain the different classes of pipeline hazards with examples in detail. How data hazards are minimized using data forwarding in a 5-stage pipeline architecture? Explain with an Example. **(16)**

Q4 What is a cache memory? Explain the various mapping techniques of cache memory. A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format? **(16)**

Q5 Describe Flynn's classification of computer architecture. Compare the features of Array Processor and Vector Processors. **(16)**

Q6 What is Interconnection network? Compare and contrast between static and dynamic networks. Draw a Shuffle network and explain the communication mechanism. **(16)**